On the FPGA-Based LWA Receiver for the J-ARGUS project: Digital Signal Processing and Hardware Verification

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1. INTRODUCTION

- The Jicamarca-Augmented Radar for Geospace and Upper atmosphere Studies (J-ARGUS) is an effort to **expand** the Jicamarca Radio Observatory (JRO) radar from a **monostatic to a tristatic configuration.**
- J-ARGUS is an international collaborative effort between UT Dallas, Geophysical Institute of Peru (IGP), Pontifical Catholic University of Peru (PUCP), Leibniz Institute of Atmospheric Physics (IAP), Cornell University, the US Air Force Research Laboratory (AFRL), and the University of New Mexico (UNM).
- J-ARGUS will advance the observational capabilities of JRO and will **benefit various areas of research, including, but not limited to, meteor science, ionospheric irregularities, ionospheric electrodynamics, and meteor afterglows**. Additionally, the system will expand JRO's services to the field of radio astronomy.
- J-ARGUS development is supported by the Major Research Instrumentation (MRI) Program of the National Science Foundation (NSF) with cost-share contributions from UTD, IGP, PUCP, Cornell University and IAP.

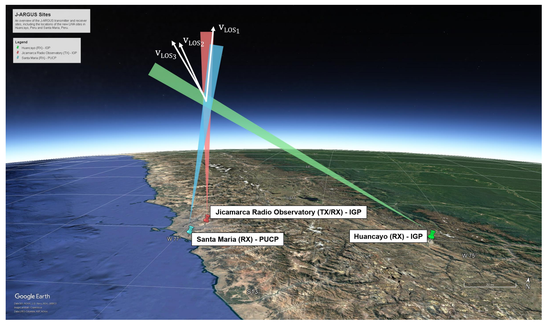

Figure 1. Sketch of the J-ARGUS system in tristatic configuration. New receive-only wideband stations are being developed based on **the Long Wavelength Array (LWA)** radio telescope architecture [1]. One station has already started to be deployed at **Huancayo, Peru**. Another station will start to be deployed at **Santa Maria, Peru** in the second semester of 2026. The existing radar infrastructure of the JRO will be used as a transmit/receive station.

Figure 2. Aerial view of the LWA antennas deployed in Huancayo, Peru. A shelter enclosure will be deployed in the circled area to house the electronics comprising the analog and Digital Signal Processing (DSP) pipeline for J-ARGUS.

2. OBJECTIVES

(OBJ 1) To **provide an overview of the J-ARGUS signal processing pipeline**, focusing specifically on the **custom interface** between the Digitizer boards - developed by the UNM - and AMD Xilinx ZCU102 boards.

(OBJ 2) To **present undergraduate student progress** towards **designing the custom interface** and using the design to **identify potential hardware faults** in the Digitizer and ZCU102 boards before they are shipped to Peru.

3. SYSTEM ARCHITECTURE

- As shown in **Figure 3(a)**, received signals in the J-ARGUS system are processed across four primary hardware domains. A critical stage of this signal path bridges the analog and digital domains via the interface between the Digitizer and ZCU102 boards, detailed in **Figure 3(b)**.

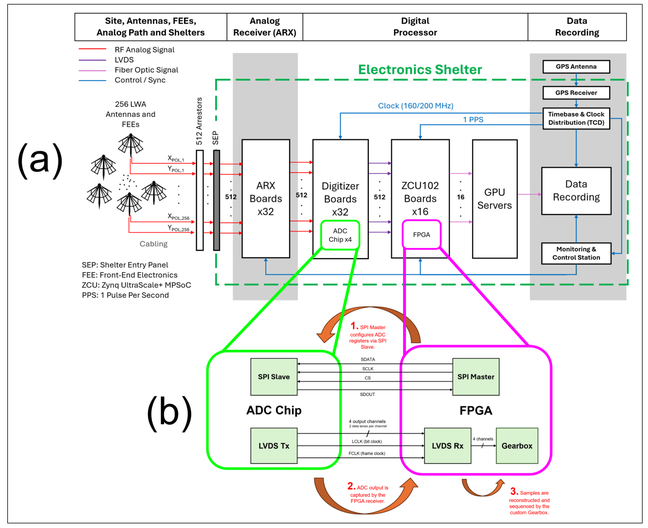

Figure 3. J-ARGUS system architecture and digitization interface. **(a)** Signal path overview: analog signals from the LWA antenna/FEE board are conditioned by the Analog Receiver, sampled by the Digitizer, preprocessed by the ZCU102 FPGA, and streamed to GPU servers and data storage for remote processing. Architecture adapted from [1]. **(b)** FPGA-to-ADC hardware interface: (1) the FPGA configures a single ADC chip via SPI; (2) the ADC streams interleaved **LVDS** data samples captured by the FPGA using the ADC **bit clock**; and (3) a custom HDL "gearbox" utilizes the ADC **frame clock** to reconstruct and sequence deserialized samples.

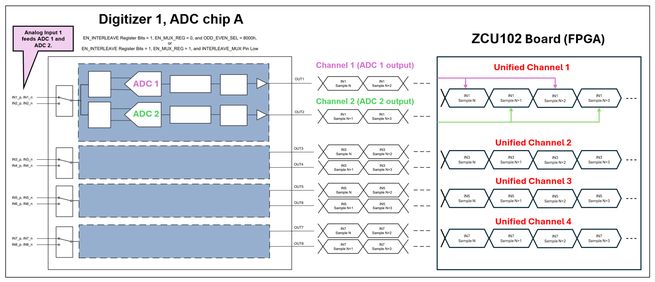

Figure 4. Configuration and operation of a single ADC chip in **interleaving-mode** with **odd inputs selected**. Eight internal conversion channels operate in pairs to digitize consecutive samples in parallel (e.g., channel 1 converts sample N, channel 2 converts sample $N+1$, etc.). The ZCU102 board sequences parallel samples into a unified channel/stream. Adapted from [2].

4. HARDWARE TEST METHODOLOGY

- **Baseline Evaluation:** Verify basic ZCU102 functionality using the manufacturer-provided AMD Built-In Self Test (BIST).
- **Custom Hardware Verification:** Because the J-ARGUS Digitizer boards are custom-designed and not mass-manufactured, they require dedicated testing platform to identify operational faults. Utilizing a Digitizer-to-ZCU102 radar-mode interface design as shown in **Figure 3(b)** serves the dual purpose of aiding system development and providing a realistic hardware-verification platform.
- **Digitizer Configuration Testing:** Configuration and clock generation testing serves as the preferred preliminary method, offering a quick, simple assessment of a Digitizer board's functional integrity. This is achieved by configuring a single ADC chip on a Digitizer board (Step 1, **Figure 3(b)**), reading back its configuration registers, and capturing/verifying the frequency of its output clocks. **With a 160 MHz input clock in interleaving-mode, correct operation yields a 480 MHz bit clock and an 80 MHz frame clock as outputs**.

5. RESULTS

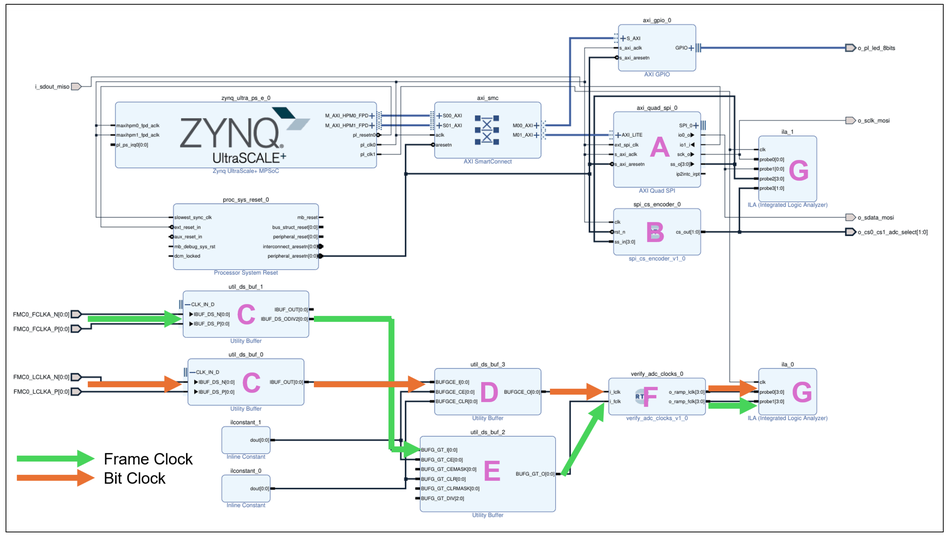

Figure 5. Synthesizable block design made with AMD's Vivado Design Suite for the ZCU102 board's FPGA. This design configures a Digitizer board ADC chip and captures/visualizes its output frame and bit clock signals. Key modules include: (A) SPI Master, (B) custom SPI Chip Select encoder, (C) differential input buffers, (D) global clock buffer, (E) global clock buffer/divider, (F) custom sawtooth generator, and (G) integrated logic analyzers (ILAs).

- After validating the ZCU102 boards via Built-In Self Test, we implemented the configuration portion of the FPGA-Digitizer interface as shown above. This design, paired with a C driver, tests basic Digitizer functionality; sample results are displayed in **Figure 6** and **Figure 7**. The test results across all boards are summarized in **Table 1**.

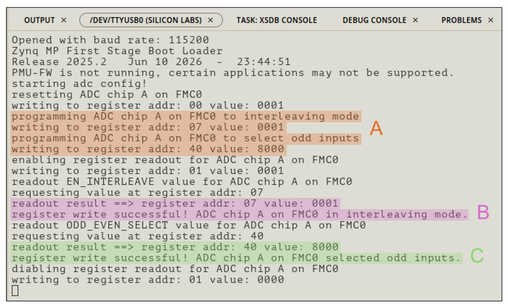

Figure 6. Serial monitor output from the driver program. Following ADC register programming (A), a read of address 0x07 returns 0x0001 (B), indicating interleaving-mode is enabled. Similarly, a read of address 0x40 returns 0x8000 (C), confirming odd analog inputs are selected.

Board Type	Total Count	Pass Count	Pass %
ZCU102	34	34	100%
Digitizer	72	69	96%

Table 1. Summary of the boards that passed preliminary tests by total count and percentage.

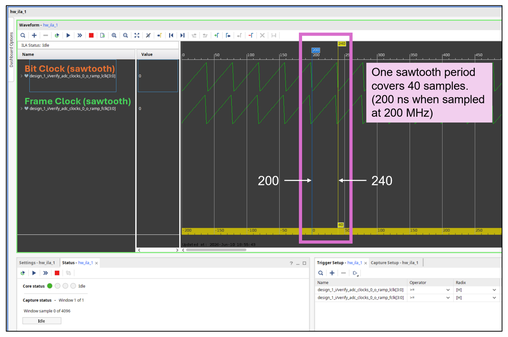

Figure 7. ILA visualization of the ADC output clocks as sawtooth waves. To prevent beating artifacts, the bit clock is divided by 6, and both clocks drive 4-bit counters to generate the sawtooth shapes. Following the phase accumulator formula ($f_{\text{out}} = \frac{f_{\text{in}}}{2^4}$), the expected frequency for both signals is 5 MHz. The observed 200 ns period confirms correct generation.

6. CONCLUSIONS

- **Custom Interface Progress (OBJ 1, OBJ 2):** The Digitizer-to-ZCU102 interface comprises the three steps detailed in **Figure 3(b)**. A student-developed FPGA block design (**Figure 5**) fully implements Step 1 and captures ADC output clocks for Step 2. Ongoing development to fully implement Steps 2 and 3 is outlined in Section 7.
- **Hardware Fault Identification (OBJ 2):** Preliminary testing revealed a 4% board failure rate (3 units) during interleaving-mode clock generation (**Table 1**). Current methods do not evaluate Digitizer data channels, so a more comprehensive testbench (**Figure 8**) leveraging the full custom interface is in development to prevent delays and costs from errors in the field after shipment to Peru.

7. ONGOING WORK

- The testbench hardware required to evaluate the Digitizer data channels is already assembled as shown in **Figure 8**. Current FPGA development focuses on Steps 2 and 3 of the interface, utilizing the AMD SelectIO Wizard and a custom HDL gearbox.

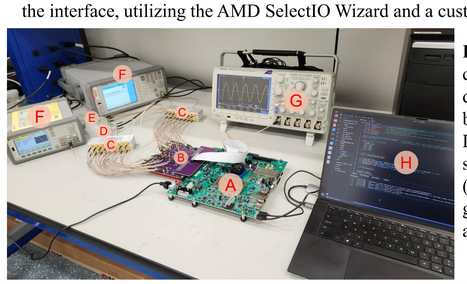

Figure 8. Lab setup for a comprehensive test of Digitizer data channels. (A) ZCU102 board, (B) Digitizer boards and Daughter board, (C) 16-way RF splitters, (D) 2-way RF splitter, (E) 4-way RF splitter, (F) signal generators, (G) oscilloscope, and (H) development laptop.

ACKNOWLEDGEMENTS

- J-ARGUS development has been supported by the NSF MRI Program (Award AGS 2215567).

REFERENCES

[1] J. Dowell and G. B. Taylor, "LWA-SV Station Architecture," Long Wavelength Array (LWA), Ver. 1, Aug. 31, 2020.
[2] ADS5296A 10-Bit, 200-MSPS, 4-Channel and 12-Bit, 80-MSPS, 8-Channel Analog-to-Digital Converter, Document No. SBAS631, Texas Instruments, Dallas, TX, USA, Oct. 2013, Revised Oct. 2025.