JRO digital receiver modernization: PCB design with an SDR approach

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Abstract

The latest data acquisition system running at the Jicamarca Radio Observatory for the main radar has been used for more than six years now. Although there are no major inconveniences on the performance there have been some problems with internal interferences which are usually unpredictable and related to the PCB design. Because of this we believe there are some chances of improvement on developing a new design. We propose a new design for the digital receivers with an SDR-like approach, this will let us manage all the data directly from the ADC which wasn't possible on the previous design. All the digital processing will be made inside an FPGA. This poster will explain in summary the different parts of the PCB design and the choices we made to improve the performance, it has been more carefully designed taking into account all possible sources of interference and signal integrity too.

1. Introduction

The new digital receiver board contemplates implementing digital signal processing stages within the FPGA to perform quadrature demodulation, filtering and decimation of the signal, as is usually done in SDR devices. A block diagram of this design is shown on Figure 1.

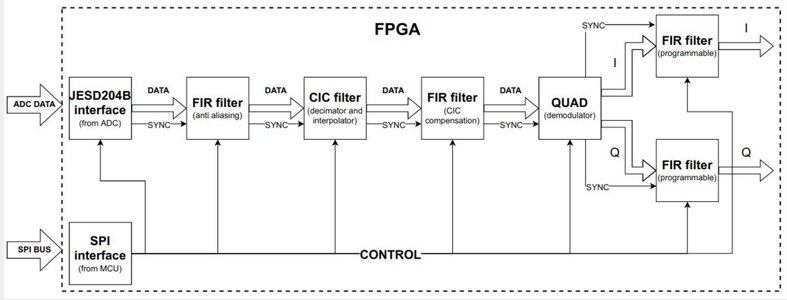

Figure 1. FPGA design for digital receiver

2. PCB design

The receiver design is separated in multiple sections:

- Power supply: To reduce any source of interference for the analog section we have selected very low noise voltage regulators with active filters to reduce any power supply noise. We can see the circuit in Figure 3.
- FPGA module: We are using the most cost effective option that can handle the GTX transceivers for the high speed JESD204B interface for the FPGA, which is the Kintex 7 FPGA.
- ADC circuit: We are using the AD9250, a dual channel 250 MSPS ADC from Analog Devices with a high speed digital interface called JESD204B. We've separated the analog circuit from the digital circuit and we included an RF shield on the PCB.
- Microcontroller: It is very common for modern FPGAs to have a small processor inside the package, despite this, we've decided to use an external microcontroller to reduce the power consumption on the FPGA, so we can focus on the DSP operations, and to be able to use a very friendly programming platform as Arduino.

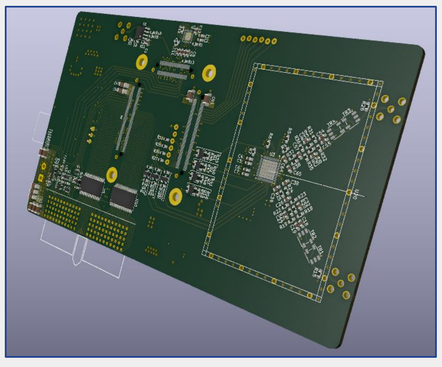

Figure 2. 3D view of the PCB design

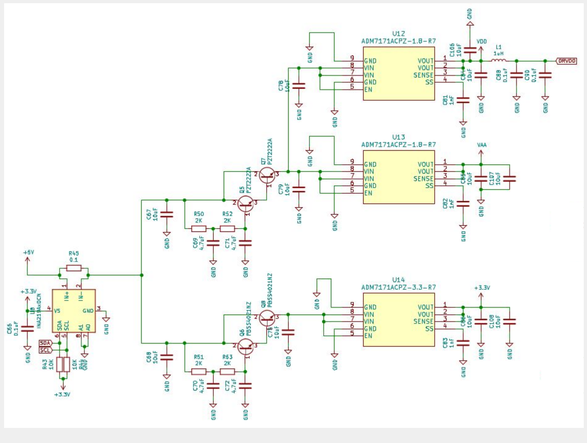

Figure 3. Voltage regulators and active filters

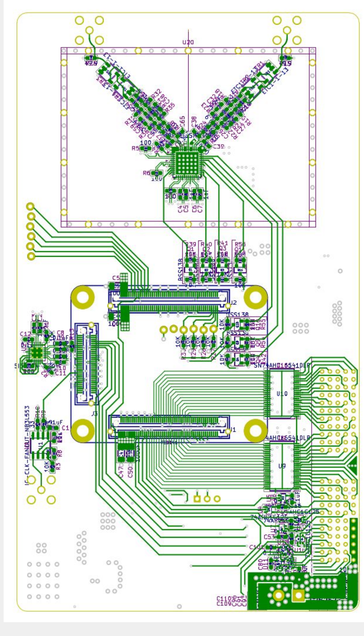

Figure 4. Bottom view of the PCB design

3. Preliminary tests with a development board

We've acquire two evaluation boards to make some tests a Kintex-7 FPGA evaluation board and an AD9250 evaluation board. We used the Vivado tool from Xilinx and a USB connection for the acquisition. Modifying the examples provided by Analog Devices we got to test the ADC with a 220 MSPS data rate, a 49.9 MHz @5 mVpp (-42 dBm) signal, which is the carrier frequency of the Jicamarca radar, and we got very promising results

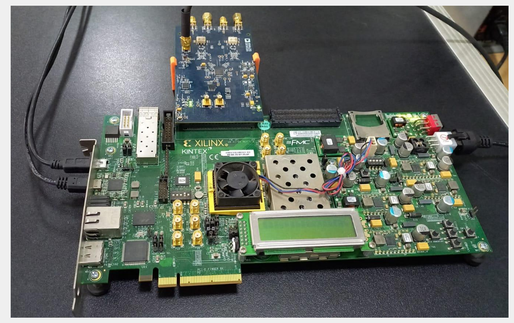

Figure 5. Xilinx Kintex-7 FPGA KC705 Evaluation board with AD9250-250EBZ

4. Results

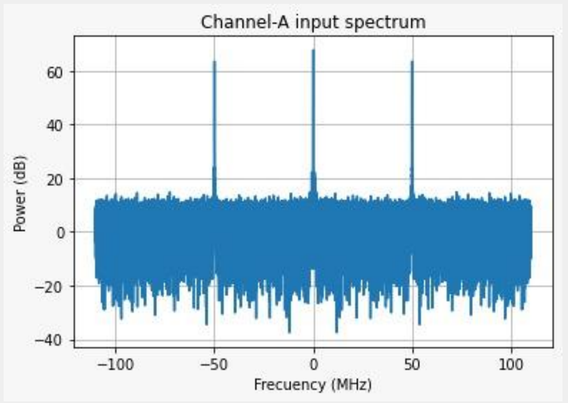

Figure 6. AD9250 49.92MHz spectral plot

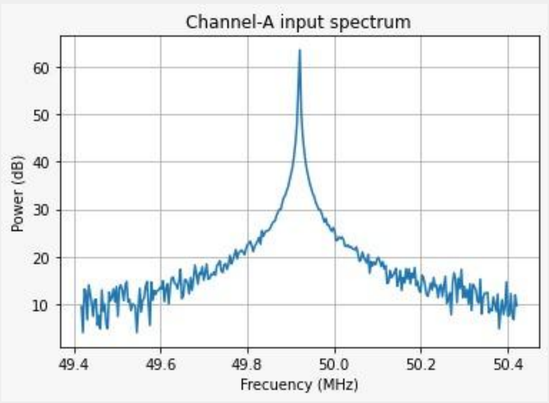

Figure 7. AD9250 49.92MHz spectral plot

In Figure 6 we can see the spectral plot with 65536 points of a 49.92 MHz signal. We've used a very small signal in order to get closer to the noise floor and see with more detail the influence of any interference on the signal. We can see a zoomed window on Figure 7 centered at 49.92 MHz. As we can see in both plots the ADC is very reliable for our application, we can't see any major interference outside DC level. We can expect even better results with our new design which is more careful with external noise.

5. Acknowledgement

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6. References

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